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NTE875
Integrated Circuit
Video IF Amplifier/PLL Detector System

Description:

The NTE875 is a complete video IF signal processing system on a single 28–Lead DIP type package. This device contains a 5–stage gain–controlled IF amplifier, a PLL synchronous amplitude detector, self–contained gated AGC, and a switchable AFC detector. The increased flexibility of the NTE875 makes it suitable for a wide variety of television applications where high quality video or sound carier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9MHz, 45.75MHz, 58.75MHz, and 61.25MHz.

Features:

- Low Differential Gain and Phase
- IF and Detector pin Compatible with NTE878 (Discontinued)
- Common–Base IF Inputs for SAW Filters
- True Synchronous Video Detector using PLL (Phase Lock Loop)
- Excellent Stability at High System Gains
- Noise–Average Gated AGC System
- Uncommitted AGC Comparator Input
- Internal AGC Gate Generator
- Superior Small–Signal Detector Linearity
- AFC Detector with Adjustable Output Bias
- 9MHz Video Bandwidth
- Reverse Tuner AGC Output

Absolute Maximum Ratings:

Power Supply Voltage, V_2 . . . . . 15V
IF Supply Current, I_5 . . . . . 60mA
AGC Gate Voltage, V_{14} . . . . . ±5V
Video Output Current, I_{16} 10mA
Phase Lock Loop (PLL) Filter Current, I_{18} 5mA
Detector Input Signal, ν_{DET} . . . . . $1V_{rms}$
Power Dissipation, P_D 2W
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 50°C/W
Junction Temperature, T_J . . . . . +125°C
Operating Temperature Range, T_{opr} . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

DC Electrical Characteristics: (T_A = +25°C, V_{IF} = v_{DET} = 0, V_{PH} = 4V, V_{COMP} = 4V, and all switches in position 0 (open) unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
12V Supply Current	$I_1 + I_2$	V_{AGC} = 6.7V, V_{COMP} = 6V	35	60	80	mA
IF Regulator Voltage	V_5	V_{AGC} = 6.7V, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage	V_7, V_8	V_{AGC} = 2V, SW2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset	$V_6 – V_9$	V_{AGC} = 2V, SW2, 3, 4 Position 1	–	0	±30	mV
IF Peaker Voltage (Max Gain)	V_3, V_4	V_{AGC} = 2V, SW2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current	I_1	V_{AGC} = 9V, SW2, 3, 4 Position 1, Measure V_1, $I_1 = (12 – V_1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain)	V_3, V_4	V_{AGC} = 9V, SW2, 3, 4 Position 1	5.5	6.2	–	V
Detector Input Voltage	V_{28}	V_{AGC} = 6.7V, SW1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage	V_{24}, V_{25}	V_{AGC} = 6.7V, SW1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage	V_{23}, V_{26}	V_{AGC} = 6.7V, SW1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage	V_{19}, V_{20}	V_{AGC} = 6.7V, SW1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold	V_{17}	SW1, 2 Position 1, Adjust V_{COMP} for I_{13} = 0	3.8	4.0	4.2	V
AGC Filter Leakage Current	I_{13}	SW1, 2, 4 Position 1	–	0	±5	µA
AGC Filter Charge Current	I_{13}	SW1, 2 Position 1, V_{COMP} = 3.5V	1.6	2.2	2.8	mA
AGC Filter Discharge Current	I_{13}	SW1, 2 Position 1, V_{COMP} = 4.5V	–0.45	–0.70	–0.90	mA
RF AGC Leakage Current	I_{11}	V_{AGC} = 2V, All Switches Position 1, Measure V_{11}, $I_{11} = (12 – V_{11})/6000$	–	0	20	µA
RF AGC Output Current	I_{11}	V_{AGC} = 10V, All Switches Position 1, Measure V_{11}, $I_{11} = (12 – V_{11})/6000$	1.5	1.8	–	mA

Detector AC Set–Up Procedure: (SW1, 4 position 1, V_{AGC} = 0V)

1. Apply v_{DET} = 10mV_{rms}, 45.75MHz CW at the detector input. Tune L1 for maximum AC signal at Pin25, measured with a 10x FET probe or through a 1pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60mV_{rms}. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output Pin16.
3. With the detector locked, adjust L3 for 4V at Pin18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring Pin16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at Pin27 (on sensitive slope of AFC curve).

AC Electrical Characteristics: (T_A = +25°C, Detector set–up as above, f = 45.75MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and allswitches in position 0 (open) unless otherwise specified)

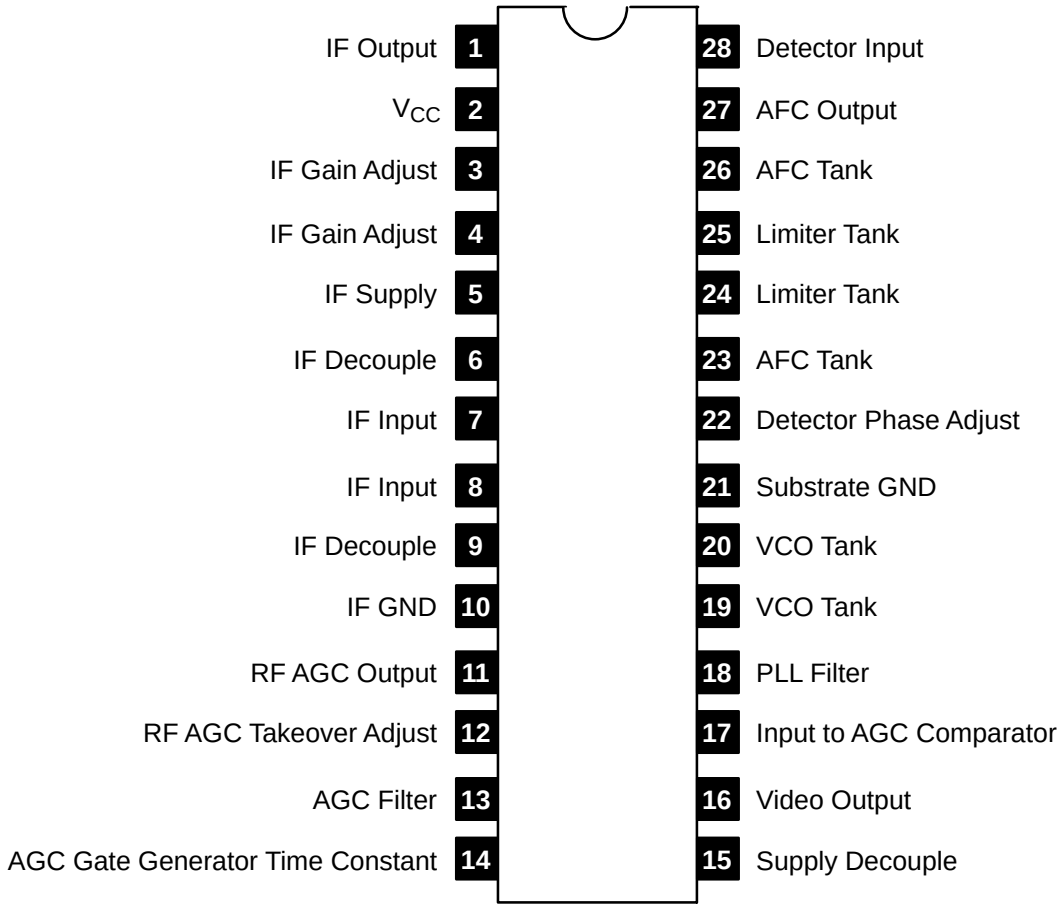
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IF Amplifier Gain	v_{OUT}/v_{IF}	V_{AGC} = 2V, SW2, 3, 4 Position 1, v_{IF} = 500µV_{rms}, Note 1	25	35	–	dB
V_{AGC} for 15dB Gain Reduction		SW2, 3, 4 Position 1, v_{IF} = 2.8mV_{rms}, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45dB Gain Reduction		SW2, 3, 4 Position 1, v_{IF} = 89mV_{rms}, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V

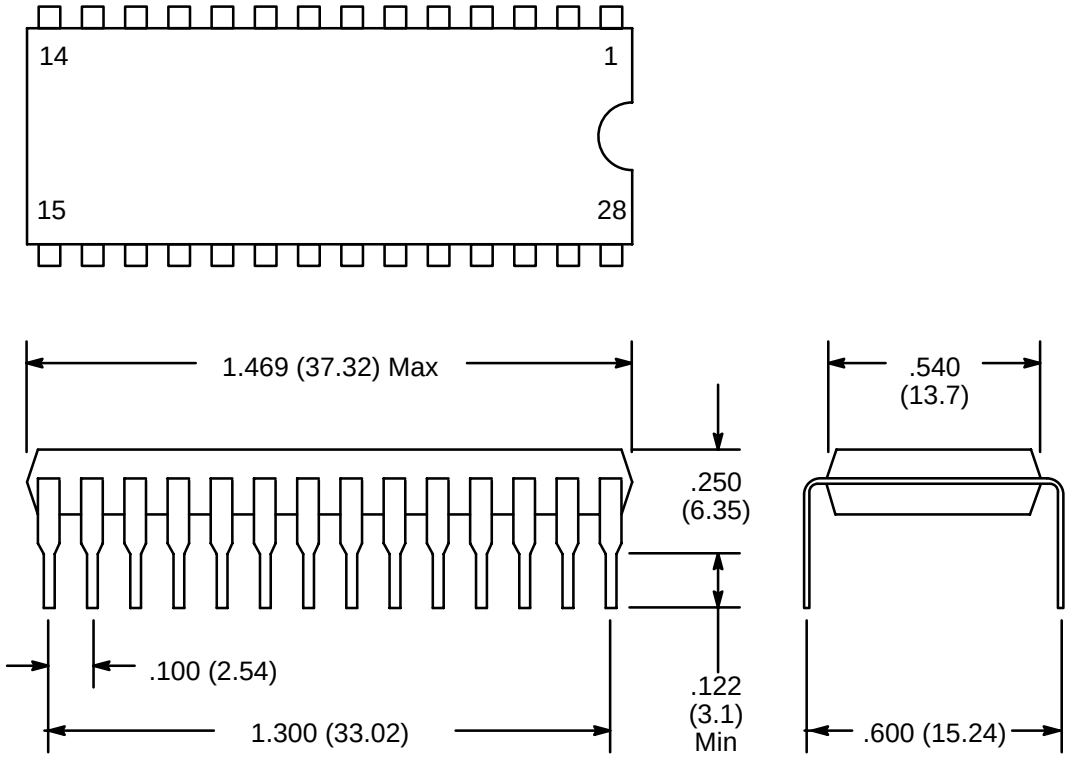
AC Electrical Characteristics (Cont'd): (T_A = +25°C, Detector set–up as above, f = 45.75MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and allswitches in position 0 (open) unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero Carrier Level	V_{16}	SW1, 2, 4 Position 1, v_{DET} = 0	6.6	7.4	8.4	V
Detected Output Level	ΔV_{16}	SW1, 2, 4 Position 1, v_{DET} = 60mV$_{rms}$, Measure Change in V_{16} from Zero Carrier Test	2.0	3.0	4.3	V
Overload Output Voltage	V_{16}	SW1, 2, 4 Position 1, v_{DET} = 600mV$_{rms}$	–	2	3	V
AFC Output Voltage (OFF)	V_{27}	SW1, 2, 4 Position 1, v_{DET} = 0	2.8	3.0	3.2	V
AFC Minimum Output Voltage	V_{27}	SW1, 4 Position 1, v_{DET} = 60mV$_{rms}$, 46.75MHz	–	0.5	1.0	V
AFC Maximum Output Voltage	V_{27}	SW1, 4 Position 1, v_{DET} = 60mV$_{rms}$, 44.75MHz	9	10	–	V
PLL Pull–In Range	Δf	SW1, 4 POsition 1, v_{DET} = 60mV$_{rms}$, Vary Frequency and Measure the Difference between Lock Points	2	3	–	MHz

Note 1. The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26dB higher.

Pin Connection Diagram




14
1
15
28
1.469 (37.32) Max
.250
(6.35)
.100 (2.54)
1.300 (33.02)
.122
(3.1)
Min
.540
(13.7)
.600 (15.24)