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NTE7049
Integrated Circuit
CMOS–Sync Generator for TV & Video Processing Systems

Description:

The NTE7049 is a CMOS LSI sync generator in a 24–Lead DIP type package that produces all the timing signals required to drive a fully 2–to–1 interlaced 525–line 30–frame/second, or 625–line 25–frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half–width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

The NTE7049 can be operated either in “genlock” mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in “stand–alone” mode, in which it is synchronized with a local on–chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train and automatically select the “genlock” or “stand–alone” mode.

A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval.

Features:

- Interlaced Composite Sync Output
- Automatic Genlock Capability
- Crystal Oscillator Operation
- 525 or 625 Line Operation
- Vertical Reset Option
- Wide Power Supply Operating Voltage: 4V to 15V

Applications:

- Cameras
- Monitors and Displays
- CATV
- Teletext
- Video Games
- Sync Restorer
- Video Service Instruments

Absolute Maximum Ratings:

DC Supply Voltage (Voltage referenced to V_{SS} terminal), V_{DD} 15V
Input Voltage Range (All Inputs), V_I . . . . . $V_{SS} \le V_I \le V_{DD}$
DC Input Current (Any One Input), I_I . . . . . ±10mA
Power Dissipation (T_A = –40° to +60°C), P_D 500mW
Derate Linearly Above +60°C to 200mW . . . . . 12mW/°C
Device Dissipation Per Output Transistor (T_A = –40° to +85°C) 100mW
Operating Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/16 ±1/32 from case for 10sec), T_L . . . . . +265°C

Static Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Quiescent Device Current	I_{DD}	V_{DD} = 5V		0.5	0.75	1.0	mA
		V_{DD} = 10V		1.5	2.0	2.5	mA
		V_{DD} = 15V		3.0	4.0	5.0	mA
Output Voltage, Low Level	V_{OL}	V_{DD} = 5V		–	–	0.01	V
		V_{DD} = 10V		–	–	0.01	V
Output Voltage, High Level	V_{OH}	V_{DD} = 5V		4.99	–	–	V
		V_{DD} = 10V		9.99	–	–	V
Threshold Voltage, N–Channel	$V_{TH}N$	I_D = 10µA		1.0	1.5	2.6	V
Threshold Voltage, P–Channel	$V_{TH}P$	I_D = 10µA		–1.0	–1.5	–2.6	V
Noise Immunity (Any Input) Low Level	V_{NL}	V_{DD} = 5V		1.5	2.25	–	V
		V_{DD} = 10V		3.0	4.5	–	V
High Level	V_{NH}	V_{DD} = 5V		1.5	2.25	–	V
		V_{DD} = 10V		3.0	4.5	–	V
Output SINK Current, N–Channel	I_DN	V_{DD} = 5V	V_O = 0.5V	80	160	–	µA
			V_O = 5V	960	1920	–	µA
		V_{DD} = 10V	V_O = 0.5V	200	400	–	µA
			V_O = 10V	2400	4800	–	µA
Output SOURCE Current, P–Channel	I_DP	V_{DD} = 5V	V_O = 4.5V	80	160	–	µA
			V_O = 0V	960	1920	–	µA
		V_{DD} = 10V	V_O = 9.5V	200	400	–	µA
			V_O = 0V	2400	4800	–	µA
Input Current (Each Input)	I_I			–	10	–	pA

Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 15pF, Note 1 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output State Propagation Delay Time (50% to 50%) Low–to–High Level	t_{PLH}	V_{DD} = 5V	–	40	80	ns
High–to–Low Level	t_{PHL}	V_{DD} = 10V	–	20	40	ns
Transition Time (10% to 90%) Low–to–High	t_{TLH}	V_{DD} = 5V	–	45	90	ns
High–to–Low	t_{THL}	V_{DD} = 10V	–	30	60	ns
Input Capacity (Per Input)	C_I		–	5	–	pF

Note 1. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

Pin Connection Diagram