ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE7001
Integrated Circuit
Horizontal Combination Circuit for Color TV & Computer Monitors

Description:

The NTE7001 is a monolithic integrated circuit in a 16–Lead DIP type package intended for use in color television receivers.

Features:

- Horizontal Oscillation Based on the Threshold Switching Principle
- Phase Comparasion Between Sync Pulse and Oscillator Voltage (φ_1)
- Internal Key Pulse for Phase Detector (φ_1) (Additional Noise Limiting)
- Phase Comparison Between Line Flyback Pulse and Oscillator Volatge (φ_2)
- Larger Catching Range Obtained by Coincidence Detector (φ_3; Between Sync and Key Pulse)
- Switch for Changing the Filter Characteristic and the Gtae Circuit (VCR Operation)
- Sync Separator
- Noise Separator
- Vertical Sync Separator and Output Stage
- Color Burst Keying and Line Flyback Blanking Pulse Generator
- Phase Shifter for the Output Pulse
- Output Pulse Duration Switching
- Output Stage with Separate Supply Voltage for Direct Drive of Thyristor Deflection Circuits
- Low Supply Voltage Protection

Applications:

- Video Monitors
- TV Receivers

Absolute Maximum Ratings:

Supply Voltage
- at Pin1 (Voltage Source), $V_{1–16}$ 13.2V
- at Pin2, $V_{2–16}$ 18V

Voltages
- Pin4, $V_{4–16}$ 13.2V
- Pin9, $\pm V_{9–16}$ 6V
- Pin10, $\pm V_{10–16}$ 6V
- Pin11, $V_{11–16}$ 13.2V

Absolute Maximum Ratings (Cont'd):

Currents

Pin2 and Pin3 (Thyristor Driving, Peak Value), I_{2M}, $-I_{3M}$ 650mA
Pin2 and Pin3 (Transistor Driving, Peak Value), I_{2M}, $-I_{3M}$ 400mA
Pin4, I_4 . . . . . 1mA
Pin6, $\pm I_6$ 10mA
Pin7, $-I_7$ 10mA
Pin11, I_{11} 2mA

Total Power Dissipation, P_{TOT} 800mW

Operating Ambient Temperature Range, T_A . . . . . –20° to +70°C

Storage Temperature Range, T_{stg} . . . . . –25°C to +125°C

DC and AC Electrical Characteristics: (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Sync Separator						
Input Switch Voltage	$V_{9–16}$		–	0.8	–	V
Input Keying Current	I_9		5	–	100	µA
Input Leakage Current	I_9	$V_{9–16}$ = –5V	–	–	1	µA
Input Switching Current	I_9		–	–	5	µA
Switch OFF Current	I_9		100	150	–	µA
Input Signal (Peak–to–Peak Value)	$V_{9–16(P–P)}$	Note 1	3	–	4	V
Noise Separator						
Input Switching Voltage	$V_{10–16}$		–	1.4	–	V
Input Keying Current	I_{10}		5	–	100	µA
Input Switching Current	I_{10}		100	150	–	µA
Input Leakage Current	I_{10}	$V_{10–16}$ = –5V	–	–	1	µA
Input Signal (Peak–to–Peak Value)	$V_{10–16(P–P)}$	Note 1	3	–	4	V
Permissible Superimposed Noise Signal (Peak–to–Peak Value)	$V_{10–16(P–P)}$		–	–	7	V
Line Flyback Pulse						
Input Current	I_6		0.02	1	2	mA
Input Switching Voltage	$V_{6–16}$		–	1.4	–	V
Input Limiting Voltage	$V_{6–16}$		–0.7	–	+1.4	V
Switching on VCR						
Input Voltage	$V_{11–16}$		0 to 2.5			V
			9 to $V_{1–16}$			V
Input Current	$-I_{11}$		–	–	200	µA
	I_{11}		–	–	2	mA
Pulse Duration Switch [t = 7µs (Thyristor Driving)]						
Input Voltage	$V_{4–16}$		–	9.4 to $V_{1–16}$		V
Input Current	I_4		200	–	–	µA
Pulse Duration Switch [t = 14µs + t_D (Transistor Driving)]						
Input Voltage	$V_{4–16}$		0	–	3.5	V
Input Current	$-I_4$		200	–	–	µA

Note 1. Permissible Range 1V to 7V.

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse Duration Switch (t = 0, $V_{3–16}$ = 0 or Input Pin4 Open)						
Input Voltage	$V_{4–16}$		5.4	–	6.6	V
Input Current	I_4		–	0	0	µA
Vertical Sync Pulse (Positive–Going)						
Output Voltage (Peak–to–Peak Value)	$V_{8–16(P–P)}$		10	11	–	V
Output Resistance	R_8		–	2	–	kΩ
Delay Between Leading Edge of Input and Output Signal	t_{ON}		–	15	–	µs
Delay Between Trailing Edge of Input and Output Signal	t_{OFF}		–	t_{ON}	–	µs
Burst Gating Pulse (Positive–Going)						
Output Voltage (Peak–to–Peak Value)	$V_{7–16(P–P)}$		10	11	–	V
Output Resistance	R_7		–	70	–	Ω
Pulse Duration	t_p	$V_{7–16}$ = 7V	– 3.7	4.0 4.3	– –	µs µs
Phase Relation Between Middle of Sync Pulse at the Input and the Leading Edge of the Burst Gating Pulse	t	$V_{7–16}$ = 7V	2.15	2.65	3.15	µs
Output Trailing Edge Current	I_7		–	2	–	mA
Line Flyback–Blanking Pulse (Positive–Going)						
Output Voltage (Peak–to–Peak Value)	$V_{7–16(P–P)}$		4	5	–	V
Output Resistance	R_7		–	70	–	Ω
Output Trailing Edge Current	I_7		–	2	–	mA
Line Drive Pulse (Positive–Going)						
Output Voltage (Peak–to–Peak Value)	$V_{3–16(P–P)}$		–	10.5	–	V
Output Resistance for Leading Edge of Line Pulse	R_3		–	2.5	–	Ω
Output Resistance for Trailing Edge of Line Pulse	R_3		–	20	–	Ω
Pulse Duration (Thyristor Driving)	t_p	$V_{4–16}$ = 9.4 to $V_{1–16}$V	5.5	7.0	8.5	µs
Pulse Duration (Transistor Driving)	t_p	$V_{4–16}$ = 0 to 4V, t_{FP} = 12µs, Note 2	–	14 + t_D	–	µs
Supply Voltage for Switching OFF the Output Pulse	$V_{1–16}$		–	4	–	V
Overall Phase Relation						
Phase Relation Between Middle of Sync Pulse and the Middle of the Flyback Pulse	t	Note 3	–	2.6	–	µs
Tolerance of Phase Relation	$\|\Delta t\|$		–	–	0.7	µs
The Adjustment of the Overall Phase Relation and Consequently the Leading Edge of the Line Drive Occurs Automatically by Phase Control φ_2. If Additional Adjustment is Applied it can be Arranged by Current Supply at Pin5.	$\Delta I_5/\Delta t$		–	30	–	µA/µs

Note 2. t_D = Switch–OFF Delay of Line Output Stage.

Note 3. Line Flyback Pulse Duration t_{FP} = 12µs.

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Threshold Voltage Low Level	V_{14-16}		–	4.4	–	V
Threshold Voltage High Level	V_{14-16}		–	7.6	–	V
Discharge Current	$\pm I_{14}$		–	0.47	–	mA
Frequency; Free Running	f_O	C_{OSC} = 4.7nF, R_{OSC} = 12kΩ	–	15.625	–	kHz
Spread of Frequency	$\Delta f_O/f_O$	Note 4	–	< ±5	–	%
Frequency Control Sensitivity	$\Delta f_O/\Delta I_{15}$		–	31	–	Hz/µA
Adjustment Range of Network in Circuit	$\Delta f_O/f_O$		–	±10	–	%
Influence of Supply Voltage on Frequency	$\frac{\Delta f_O/f_O}{\Delta V/V_{NOM}}$	Note 4	–	< ±0.05	–	%
Change of Frequency when V_{1-16} Drops to 5V	Δf_O	Note 4	–	< ±10	–	%
Temperature Coefficient of Oscillator Frequency		Note 4	–	< $\pm 10^{-4}$	–	Hz/°C
Phase Comparison φ_1						
Control Voltage Range	V_{13-16}		3.8	8.2	–	V
Control Current (Peak Value)	$\pm I_{13M}$		1.9	2.3	–	mA
Output Leakage Current	I_{13}	V_{13-16} = 4 to 8V	–	–	1	µA
Output Resistance	R_{13}	V_{13-16} = 4 to 8V, Note 5	High Ohmic			
		V_{13-16} < 3.8V or > 8.2V, Note 6	Low Ohmic			
Control Sensitivity			–	2	–	kHz/µs
Catching and Holding Range	Δf	82kΩ Between Pins 13 and 15	–	±780	–	Hz
Spread of Catching and Holding Range	Δ(Δf)	Note 4	–	±10	–	%
Phase Comparison φ_2 and Phase Shifter						
Control Voltage range	V_{5-16}		5.4	–	7.6	V
Control Current (Peak Value)	$\pm I_{5M}$		–	1	–	mA
Output Resistance	R_5	V_{5-16} = 5.4 to 7.6V, Note 7	–	High Ohmic		
		V_{5-16} < 5.4 or > 7.6V	–	8	–	kΩ
Input Leakage Current	I_5	V_{5-16} = 5.4 to 7.6V	–	–	5	µA
Permissible Delay Between Leading Edge of Output Pulse and Leading Edge of Flyback Pulse	t_D	t_{FP} = 12µs	–	–	15	µs
Static Control Error	$\Delta t/\Delta t_D$		–	–	0.2	%
Coincidence Detector φ_3						
Output Voltage	V_{11-16}		0.5	0	6.0	V
Output Current (Peak Value)	I_{11M}	Without Coincidence	–	0.1	–	mA
	$-I_{11M}$	With Coincidence	–	0.5	–	mA
Time Constant Switch						
Output Voltage	V_{12-16}		–	6	–	V
Output Current (Limited)	$\pm I_{12}$		–	–	1	mA
Output Resistance	R_{12}	V_{11-16} = 2.5 to 7V	–	0.1	–	kΩ
		V_{11-16} < 1.5V or > 9V	–	60	–	kΩ

DC and AC Electrical Characteristics (Cont'd): (V_{CC} = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Gating Pulse						
Pulse Duration	t_p		–	7.5	–	µs

Note 4. Excluding External Component Tolerances.

Note 5. Current Source.

Note 6. Emitter–Follower.

Note 7. Current Source.

Pin Connection Diagram