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NTE1857
Integrated Circuit
Stepper Motor Driver

Description:

The NTE1857 is designed to drive a two–phase stepper motor in the bipolar mode, The circuit of four input sections, a logic decoding/sequencing section, two driver–stages for the motor coils, and an output to indicate the Phase A drive state.

Features:

- Single Supply Operation: +7.2V to +16.5V
- 350mA/Coil Drive Capability
- Clamp Diodes Provided for Back–EMF Suppression
- Selectable $\overline{\text{CW}}$/CCW and $\overline{\text{Full}}$/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis: 400mV Min
- Phase Logic Can Be Initialized to $\overline{\text{Phase A}}$
- $\overline{\text{Phase A}}$ Output Drive State Indication (Open–Collector)

Input Truth Table:

	Input Low	Input High
$\overline{\text{CW}}$/CCW	CW	CCW
$\overline{\text{Full}}$/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_M . . . . . +18V
Clamp Diode Cathode Voltage (Pin1), V_D . . . . . V_M +5.0V
Driver Output Voltage (Pins 2, 3, 14, 15), V_{OD} . . . . . V_M +6.0V
Driver Output Current/Coil, I_{OD} . . . . . ±500mA
Input Voltage (Pins 7, 8, 9, 10), V_{in} . . . . . –0.5 to +7.0V
$\overline{\text{Bias}}$/Set Current (Pin6), I_{BS} . . . . . –10mA
$\overline{\text{Phase A}}$ Output Voltage (Pin11), V_{OA} . . . . . +18V
$\overline{\text{Phase A}}$ Sink Current (Pin11), I_{OA} 20mA
Junction Temperature, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Thermal Resistance, Junction–to–Ambient (No Heat Sink), R_{thJA} . . . . . 45°C/W

Note 1. “Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The “Electrical Characteristics” tables provide conditions for actual device operation.

Recommended Operating Conditions:

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+7.2	+16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	V_M + 4.5	Vdc
Driver Output Current (Per Coil)	I_{OD}	–	350	mA
Input Voltage (Pins 7, 8, 9, 10)	V_{in}	0	+5.5	Vdc
$\overline{\text{Bias}}$/Set Current (Outputs Active)	I_{BS}	–300	–75	μA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	–	V_M	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+70	°C

DC Electrical Characteristics:

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise specified, See Notes 2, 3)

Parameter	Pins	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Logic Levels								
Threshold Voltage (Low–to–High)	7, 8, 9, 10	V_{TLH}			–	–	2.0	V
Threshold Voltage (High–to–Low)		V_{HTL}			0.8	–	–	V
Hysteresis		V_{HYS}			0.4	–	–	V
Current		I_{IL}	V_I = 0.4V		–100	–	–	μA
		I_{IH1}	V_I = 5.5V		–	–	+100	μA
		I_{IH2}	V_I = 2.7V		–	–	+20	μA
Driver Output Levels								
Output High Voltage	2, 3, 14, 15	V_{OHD}	I_{BS} = –300μA	I_{OD} = –350mA	V_M–2.0	–	–	V
				I_{OD} = –0.1mA	V_M–1.2	–	–	V
Output Low Voltage		V_{OLD}	I_{BS} = –300μA, I_{OD} = 350mA		–	–	0.8	V
Differential Mode Output Voltage Difference		DV_{OD}	I_{BS} = –300μA, I_{OD} = 350mA, Note 4		–	–	0.15	V
Common Mode Output Voltage Difference		CV_{OD}	I_{BS} = –300μA, I_{OD} = –0.1mA, Note 5		–	–	0.15	V
Output Leakage – HiZ State		I_{OZ1}	0 ≤ V_{OD} ≤ V_M	I_{BS} = –5μA	–100	–	+100	μA
		I_{OZ2}		I_{BS} = –300μA, Pin9 = 2V, Pin8 = 0.8V	–100	–	+100	μA
Clamp Diodes								
Forward Voltage	1, 2, 3, 14, 15	V_{DF}			–	2.5	3.0	V
Leakage Current (Per Diode)		I_{DR}	Pin1 = 21V, Pins 2, 3, 14, 15 = 0V, I_{BS} = 0μA		–	–	100	μA

Note 2. Algebraic convention rather than absolute values is used to designate limit values.

Note 3. Current into a pin is designated as positive. Current out of a pin is designated as negative.

Note 4. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where
$V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and
$V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.

Note 5. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC Electrical Characteristics (Cont'd): (Specifications apply over the recommended supply voltage and temperature ranges unless otherwise specified, See Notes 2, 3)

Parameter	Pins	Symbol	Test Conditions		Min	Typ	Max	Unit
$\overline{\text{Phase A}}$ Output								
Output Low Voltage	11	V_{OLA}	I_{OA} = 8mA		–	–	0.4	V
Off State Leakage Current		I_{OHA}	V_{OHA} = 16.5V		–	–	100	μA
Power Supply								
Power Supply Current	16	I_{MW}	I_{OD} = 0μA, I_{BS} = –300μA, L1 = V_{OHD}, L2 = V_{OLD}	L3 = V_{OHD}, L4 = V_{OLD}	–	–	70	mA
		I_{MZ}		L3 = HiZ, L4 = HiZ	–	–	40	mA
		I_{MN}		L3 = V_{OHD}, L4 = V_{OLD}	–	–	75	mA
$\overline{\text{Bias}}$/Set Current								
To Set $\overline{\text{Phase A}}$	6	I_{BS}			–5.0	–	–	μA

Note 2. Algebraic convention rather than absolute values is used to designate limit values.

Note 3. Current into a pin is designated as positive. Current out of a pin is designated as negative.

AC Switching Characteristics: (T_A = +25°C, V_M = 12V unless otherwise specified)

Parameter	Pins	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}		0	–	50	kHz
Clock Pulse Width – High	7	PW_{CKH}		10	–	–	μs
Clock Pulse Width – Low	7	PW_{CKL}		10	–	–	μs
$\overline{\text{Bias}}$/Set Pulse Width	6	PW_{BS}		10	–	–	μs
Setup Time – $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7, 9–7	t_{su}		5	–	–	μs
Hold Time – $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7, 9–7	t_h		10	–	–	μs
Propagation Delay – Clk–to–Driver Output		t_{PCD}		–	8	–	μs
Propagation Delay – $\overline{\text{Bias}}$/Set–to–Driver Output		t_{PBSD}		–	1	–	μs
Propagation Delay – Clk–to–$\overline{\text{Phase A}}$ Low	7–11	t_{PHLA}		–	12	–	μs
Propagation Delay – Clk–to–$\overline{\text{Phase A}}$ High	7–11	t_{PLHA}		–	5	–	μs

Pin Description:

Name	Symbol	Pin #	Description
Power Supply	V_M	16	Power supply pin for both the logic circuit and the motor coil current. Voltage is +7.2 to +16.5V.
Ground	GND	4, 5, 12, 13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
Clamp Diode Voltage	V_D	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin16.
Driver Outputs	L1, L2, L3, L4	2, 3, 14, 15	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
$\overline{\text{Bias}}$/Set	B/S	6	This pin is typically 0.7 below V_M. The current out of this pin (through a resistor to GND) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0μA) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition.
Clock	Clk	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin6 is open.

Pin Description (Cont'd):

Name	Symbol	Pin #	Description
$\overline{\text{Full}}$/Half Step	$\overline{\text{F}}$/HS	9	When low (Logic "0"), each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one−half step. See Fig. 1 for sequences.
Clockwise/ Counterclockwise	CW/CCW	10	This input allows reversing the rotation of the motor. See Fig. 1 for sequence.
Output Impedance Control	OIC	8	This input is relevant only in the half step mode (Pin9 > 2.0V). When low (Logic "0") the two driver outputs of the non−energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 1.
Phase A	Ph A	11	This open−collector output indicates (when low) that the driver outputs are in the Phase A condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

Application Information:

General

The NTE1857 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350mA to each of two coils of a two−phase motor. The outputs change state with each low−to−high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions on Pins 8, 9, and 10.

Outputs (Pins 2, 3, 14, 15)

The outputs (L1−L4) are high current outputs, which when connected to a two−phase motor, provide two full−bridge configurations. The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

The maximum sink current available at the outputs is a function of the resistor connected between Pin6 and GND (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L) of each output are off.

V_D (Pin1)

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back−EMF voltage spikes. Pin1 is normally connected to V_M (Pin16) through a diode (zener or regular), a resistor, or directly. The peak instantaneous voltage at the outputs (Pins 2, 3, 14, and 15) must not exceed V_M by more than 6 volts. The voltage drop across the internal clamping diodes must be included in design. Parasitic diodes across each Q_L of each output provide for a complete circuit path for the switched current.

$\overline{\text{Full}}$/Half Step (Pin9)

When this input is at a Logic "0" (< 0.8 volts), the outputs change a full step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin10). There are four steps (Phase A,B,C,D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step.

When taken to a Logic "1" (> 2.0 volts), the outputs change a half step with each clock cycle, with the sequence direction depending on the $\overline{\text{CW}}$/CCW input (Pin10). Eight steps (Phases A−H) result for each complete cycle of the sequencing logic. Phases A,C,E and G correspond (in polarity) to the phases A, B, C, and D, respectively, of the full step sequence. Phases B, D, F and H provide current to one motor coil, while de−energizing the other coil. The condition of the outputs of the de−energized coil depends on the OIC input (Pin8).

OIC (Pin8)

The output impedance control input determines the output impedance to the de−energized coil when operating in the half−step mode. When the outputs are in Phase B, D, F or H and this input is at a Logic "0" (< 0.8V), the two outputs to the de−energized coil are in a high−impedance condition−Q_L and Q_H of both outputs are off. When this input is at a Logic "1" (> 2.0V), a low impedance output is provided to the de−energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting Pin1 (V_D) to Pin16 (V_M) as described elsewhere in this data sheet.

$\overline{\text{Bias}}$/Set (Pin6)

This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_L's) of each output, which in turn, is a functional of I_{BS}. The appropriate value of I_{BS} is determined by;

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps. The value of R_B (between Pin6 and GND) is then determined by:

$$R_B = \frac{V_M - 0.7V}{I_{BS}}$$

b) When Pin 6 is opened (raised to V_M) such that I_{BS} is < 5.0 μA, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The Phase A output (Pin11) goes active (low), and input signals at Pins 7,8,9 and 10 are ignored (low), and input signals at Pins 7, 8, 9, and 10 are ignored during this time. Upon re−establishing I_{BS}, the driver outputs become active, and will be in the Phase A position (L1 = L3 = V_{OHD}, L2 = L4=V_{OLD}). The circuit will then respond to the inputs at Pins 7, 8, 9, and 10.

The Set function (opening Pin6) can be used as a power−up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75μA will reduce the motor current, but will not reset the internal logic as described above.

Power Dissipation

The power dissipated by the NTE1857 must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P=(V_M \times I_M) + (2 \times I_{OD}) [(V_M - V_{OHD}) + V_{OLD}]$$

where V_M = Supply voltage:
I_M = Supply current other than I_{OD}:
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

If T_J is higher than 150°C, a heat sink could be used to reduce $R_{\Theta JA}$. In extreme cases forced air cooling should be considered. It is assumed that a ground plane is provided under the NTE1857 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and I_R drops when switching the motor current.

Pin Connection Diagram

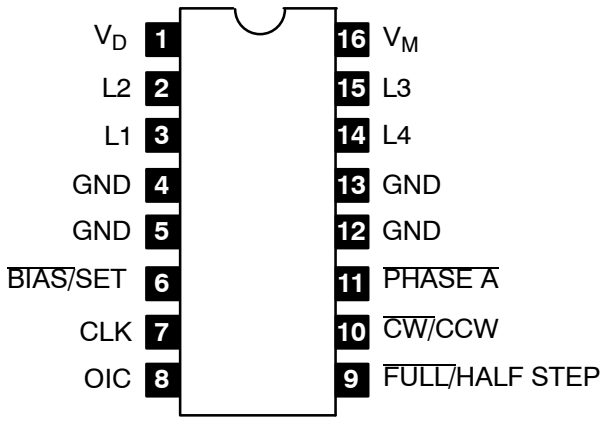

Fig. 1 – Output Sequence