ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE1722
Integrated Circuit
Pulse Width Modulator (PWM) Control Circuit

Description:

The NTE1722 is a high performance pulse width modulator integrated circuit in an 18–Lead DIP type package intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports art TTL and B–series CMOS compatible. Active low logic design allows easy wired–OR connections for maximum flexibility. The versatility of this device enables implementation in single–ended or push–pull switching regulators that are transformerless or transformer coupled.

Features:

- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0Hz to 400kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100mA
- Digital Current Limiting
- Programmable Dead Time
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

Absolute Maximum Ratings: (Values beyond which damage may occur)

Supply Voltage, V_{CC} . . . . . +40V
Collector Supply Voltage, V_C . . . . . +40V
Logic Inputs . . . . . –0.3 to +5.5V
Analog Inputs . . . . . –0.3 to V_{CC} V
Output Current (Source or Sink), I_O . . . . . ±200mA
Reference Load Current (V_{CC} = 40V, Note 1), I_{ref} 50mA
Logic Sink Current 15mA
Power Dissipation (T_A = +25°C), P_D 1000mW
Derate Above 50°C . . . . . 10mW/°C
Power Dissipation (T_C = +25°C), P_D 3000mW
Derate Above 25°C . . . . . 24mW/°C
Operating Junction Temperature, T_J . . . . . + 150°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 100°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . ±300°C

Note 1. Maximum junction temperature must be observed.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		+8.0	–	+35	V
Collector Supply Voltage	V_C		+4.5	–	+35	V
Output Sink/Source Current (Each Output)	I_O		0	–	±100	mA
Reference Load Current	I_{ref}		0	–	20	mA
Oscillator Frequency Range	I_{ref}		0	–	20	mA
Oscillator Timing Resistor	R_T		2.0	–	150	kΩ
Oscillator Timing Capacitor	C_T		0.001	–	20	µF
Available Deadtime Range (40kHz)	–		3.0	–	50	%
Operating Junction Temperature Range	T_J		0	–	+125	°C

Electrical Characteristics: (V_{CC} = 15V, T_J = 0° to +125°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Referencd Section (I_L = 0mA unless otherwise specified)						
Reference Output Voltage	V_{ref}	T_J = +25°C	4.90	5.00	5.10	V
Line Regulation	Reg_{line}	+8.0V ≤ V_{CC} ≤ +35V	–	10	30	mV
Load Regulation	Reg_{load}	0mA ≤I_L ≤ 20mA	–	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T_J$		–	10	–	mV
Total Reference Output Voltage Variation	ΔV_{ref}	+8.0V ≤ V_{CC} ≤ +35V, 0mA ≤ I_L ≤ 20mA	4.85	5.00	5.15	V
Short Circuit Current	I_{SC}	V_{ref} = 0V, Note 1	25	80	125	mA
Uundervoltage Lockout						
$\overline{\text{Reset}}$ Output Voltage	–	V_{ref} = +3.8V	–	0.2	0.4	V
		V_{ref} = +4.8V	2.4	4.8	–	V
Oscillator Section (Note 2)						
Initial Accuracy	–	T_J = +25°C	–	±3.0	±8.0	%
Frequency Stability over Power Supply Range	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	+8.0V ≤ V_{CC} ≤ +35V	–	0.5	1.0	%
Frequency Stability over Temperature	$\frac{\Delta f_{osc}}{\Delta T_J}$	ΔT_J = 0° to +125°C	–	2.0	–	%
Minimum Frequency	f_{min}	R_T = 150kΩ, C_T = 20µF	–	0.5	–	Hz
Maximum Frequency	f_{max}	R_T = 2kΩ, C_T = 0.001µF	400	–	–	kHz
Sawtooth Peak Voltage	$V_{osc(p)}$	V_{CC} = +35V	–	3.0	3.5	V
Sawtooth Valley Voltage	$V_{osc(v)}$	V_{CC} = +8V	0.45	0.8	–	V
Error Amplifier Section (0V ≤ V_{CM} ≤ +5.2V unless otherwise specified)						
Input Offset Voltage	V_{IO}	R_S ≤ 2kΩ	–	20	10	mV
Input Bias Current	I_{IB}		–	–350	–2000	nA
Input Offset Current	I_{IO}		–	35	200	nA
DC Open Loop Gain	A_{VOL}	R_L ≥ 10MΩ	60	72	–	dB

Note 1. Maximum junction temperature must be observed.
Note 2. f_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01µF ± 1%, R_D = 0Ω)

Electrical Characteristics (Cont'd): (V_{CC} = 15V, T_J = 0° to +125°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier Section (Cont'd) ($0V \le V_{CM} \le +5.2V$ unless otherwise specified)						
High Output Voltage	V_{OH}	$V_{Pin1} - V_{Pin2} \ge +150mV$, $I_{Source} = 100\mu A$	3.6	4.2	–	V
Low Output Voltage	V_{OL}	$V_{Pin2} - V_{Pin1} \ge +150mV$, $I_{Sink} = 100\mu A$	–	0.2	0.4	V
Common Mode Rejection Ratio	CMRR	$R_S \le 2k\Omega$	70	94	–	dB
Power Supply Rejection Ratio	PSRR	$+12V \le V_{CC} \le +18V$	66	80	–	dB
PWM Comparator Section (Note 2)						
Minimum Duty Cycle	DC_{min}	$V_{compensation}$ = +0.4V	–	–	0	%
Maximum Duty Cycle	DC_{max}	$V_{compensation}$ = +3.6V	45	49	–	%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, $\overline{RESET}$)						
Output Voltage, High Logic Level	V_{OH}	I_{source} = 40µA	2.4	4.0	–	V
Output Voltage, Low Logic Level	V_{OL}	I_{sink} = 3.6mA	–	0.2	0.4	V
Input Current, High Logic Level	I_{IH}	V_{IH} = +2.4V	–	–125	–200	µA
Input Current, Low Logic Level	I_{IL}	V_{IL} = +0.4V	–	–225	–360	µA
Current Limit Comparator Section ($0V \le V_{CM} \le +12V$ unless otherwise specified)						
Sense Voltage	V_{sense}	$R_S \le 50\Omega$	80	100	120	mV
Input Bias Current	I_{IB}		–	–3	–10	µA
Soft–Start Section						
Error Clamp Voltage		$\overline{Reset}$ = +0.4V	–	0.1	0.4	V
$C_{Soft–Start\ Charging\ Current}$	I_{CS}	$\overline{Reset}$ = +2.4V	50	100	150	µA
Output Drivers (Each Output, V_C = +15Vdc unless otherwise specified)						
Output High Level	V_{OH}	I_{source} = 20mA	12.5	13.5	–	V
		I_{source} = 100mA	12.0	13.0	–	V
Output Low Level	V_{OL}	I_{Sink} = 20mA	–	0.2	0.3	V
		I_{Sink} = 100mA	–	1.2	2.0	V
Collector Leakage	$I_{C(Leak)}$	V_C = +40V	–	50	150	µA
Rise Time	t_r	C_L = 1000pF	–	0.3	0.6	µs
Fall Time	t_f		–	0.1	0.2	µs
Supply Current	I_{CC}	Shutdown + +0.4V, V_{CC} = +35V, $R_T = 4.12k\Omega$	–	18	30	mA

Note 2. f_{OSC} = 40kHz ($R_T = 4.12k\Omega \pm 1\%$, $C_T = 0.01\mu F \pm 1\%$, $R_D = 0\Omega$)

Pin Connection Diagram