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NTE1167
Integrated Circuit
Phase Lock Loop (PLL) Frequency Synthesizer

Description:

The NTE1167 consists of a crystal oscillator, 10 bit divider, phase comparator, and a programmable divide–by–N 9–bit counter in a single CMOS 16–Lead DIP type integrated circuit.

This device is designed for use in frequency synthesizers and phase locked loop applications for CB transceivers since it includes a reference frequency selector pin.

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Supply Voltage, $V_{DD} – V_{SS}$ . . . . . –0.3V to +7V
Input Voltage, V_{IN} . . . . . $V_{SS} \le V_{IN} \le V_{DD}$
Power Dissipation, P_D 250mW
Operating Temperature Range, T_{opr} . . . . . –30° to +70°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C
Lead Temperature (During Soldering, 5sec Max), T_L . . . . . +260°C

Electrical Characteristics: ($V_{DD} – V_{SS}$ = 6V, –30° ≤ T_A ≤ +70°C, $f_{in} \bullet Q_{in}$ = 10.24MHz unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage (All Inputs) Low Level	V_{IL}	Note 1	–	–	0.5	V
High Level	V_{IH}		5.5	–	–	V
Pull–Up Resistance	$R_{UP} \bullet F_S$		–	2.0	0	MΩ
Pull–Down Resistance	$R_{DN} \bullet P_0 – P_8$		15	75	–	kΩ
Supply Current	I_{DD}	V_{DD} = 5.5V, $V_{in} \bullet F_{in}$ = $1V_{P–P}$, Exclude sink current of preset pin	–	5.0	9.0	mA
Output Voltage High Level	$V_{OH} \bullet LD$	I_{OH} = 0.1mA	5.5	–	–	V
Low Level	$V_{OL} \bullet LD$	I_{OL} = 0.1mA	0	–	0.5	V
Output Current High Level	$I_{SAT} \bullet H \bullet D_O$	V_O = 0V	400	–	–	µA
Low Level	$I_{SAT} \bullet L \bullet D_O$	V_O = 0V	400	–	–	µA
Output Voltage	$V_{IF} \bullet F_{in}$	V_{DD} = 5V	1.7	2.2	2.8	V
	$V_{IF} \bullet F_S$		5.5	–	–	V
	$V_{IF} \bullet P_0 – P_8$		–	–	0.5	V
Max Input Frequency	$f_{IN} \bullet$ Max Q_{in}		11	–	–	MHz
	$f_{IN} \bullet$ Max F_{in}		3.3	–	–	MHz
Max Free Running Frequency	$f_{FR} \bullet$ Max $\bullet F_{IN}$		3.5	–	–	MHz
Operating Voltage	V_{DD}		5.0	–	6.5	V

Note 1. All inputs refers to pins P_0 to P_8, F_S, F_{in}, and Q_{in}. This parameter defins their input levels at DC coupling.

Pin Connection Diagram